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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/692,957 | 10/24/2003 | Anand Pande | 14920US01 | 2011 |

23446 7590 11/14/2005

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| EXAMINER | |
|---|---|
| FRANKLIN, RICHARD B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/692,957 | PANDE, ANAND | |
| | Examiner | Art Unit | |
| | Richard Franklin | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *20-22,25 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1 – 26 have been examined.

### *Election/Restrictions*

2. Claims 20 – 22 and 25 – 26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 23 September 2005.

### *Claim Objections*

3. Claim 13 is objected to because of the following informalities:

- Claim 13: The word "pointer" is misspelled as "point" in line 2.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 is dependent on Claim 1 and claims a code generator coupled to a read pointer, which is coupled to a storage device. It is not clear if the storage device

referred to in Claim 10 is the FIFO memory of Claim 1 or a new storage device. The Examiner has interpreted the storage device as being the FIFO memory of Claim 1, as that is what is illustrated in Figure 1 of the current specification.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 4, 12 – 13, 16, and 23 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pontius US Patent No. 6,337,893 (hereinafter Pontius) in view of Yi US Patent No. 6,703,950 (hereinafter Yi).

As per claim 1, Pontius teaches a first-in-first-out (FIFO) memory having a length of d where d is an integer (Pontius; Col 4 Lines 37 – 46). Pontius also teaches generating a code sequence having a length of 2d (Pontius; Col 4 Lines 37 – 46).

Pontius does not teach that the code sequence is a first code sequence and is generated from a second code sequence by removing one or more pairs of mirrored codes from the second code sequence. The first code sequence has a circular property and a Hamming length of one for any two consecutive codes of the first code sequence.

Yi teaches producing a code sequence of any even integer length and having a circular property and a Hamming length of one for any two consecutive codes by reducing a second code sequence (Yi; Figure 3a, Table 3a) into a first code sequence

(Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored codes from the second code sequence (Yi; Figures 3a – 3b, Tables 3a – 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius to include wherein the code sequence is generated by removing one or more pairs of mirrored codes from a second code sequence to form a first code sequence that has a length of 2d, a circular property, and a Hamming length of one for any two consecutive codes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius by the teaching of Yi because including the first code sequence that is generated by removing one or more pairs of mirrored codes from a second code sequence to form a first code sequence that has a length of 2d, a circular property, and a Hamming length of one for any two consecutive codes allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 2, Pontius as modified teaches wherein the second code sequence has a circular property and a Hamming length of one for any two consecutive codes of the second code sequence (Yi; Figures 3a – 3b).

As per claim 3, Pontius as modified teaches wherein the first code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 4, Pontius as modified teaches wherein the second code sequence is a Gray-code sequence (Yi; Figures 3a – 3b).

As per claim 12, Pontius as modified inherently teaches wherein the FIFO memory comprises a write data input port and a read data input port because these ports are common on FIFO memory devices.

As per claim 13, Pontius as modified inherently teaches wherein the FIFO memory comprises a write pointer input and a read pointer input because these inputs are common on FIFO memory devices.

As per claims 16 and 23, Pontius teaches a memory of depth d in which d is not equal to a value $2^n$ and in which d and n are integers (Pontius; Col 4 Lines 37 – 46). A code sequence of length 2d is generated and used as read and write pointers to the memory (Pontius; Figure 1 Items 10 and 20, Col 4 Lines 37 – 46).

Pontius does not teach reducing a first Gray-code sequence of length $2^n$ into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-code sequences.

Yi teaches reducing a first Gray-code sequence of length $2^n$ (Yi; Figure 3a, Table 3a) into a second Gray-code sequence of length 2d (Yi; Figure 3b, Table 3b) by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence (Yi; Figures 3a – 3b, Tables 3a – 3b, and Col 4 Lines 5 – 19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius to include wherein a Gray-code sequence of length $2^n$ is reduced into a Gray-code sequence of 2d by removing one or more pairs of mirrored Gray-code sequences from the first Gray-code sequence.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius by the teaching of Yi because the reduced size of the code allows for a geometrically reduced storage requirement (Yi; Col 2 Lines 54 – 58).

As per claim 24, Pontius as modified teaches wherein at least one of the first code sequence and the second code sequence has at least one of a closed property and a Hamming distance of one (Yi; Figures 3a – 3b).

6. Claims 5 – 11, 14 – 15, and 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pontius US Patent No. 6,337,893 (hereinafter Pontius) in view of Yi US Patent No. 6,703,950 (hereinafter Yi) as applied to claims 1 – 4, 12 – 13, 16, and 23 – 24 above, and further in view of Miyamoto et al. US Patent No. 6,810,468 (hereinafter Miyamoto).

As per claim 5, Pontius as modified does not teach that the code generator is coupled to a write pointer that is in turn connected to the first-in-first-out (FIFO) memory.

Miyamoto teaches an asynchronous FIFO memory that has a code generator connected to a write pointer (Miyamoto; Figure 1 Item 21).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius as modified to include a write pointer that is connected to the code generator and the FIFO memory.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Pontius as modified by the teaching of Miyamoto because the write pointer allows for determination of asynchronous FIFO status flags without stability errors.

As per claim 6, Pontius as modified also teaches wherein the write pointer is coupled to the FIFO memory via at least one of a converter and a look-up table (Miyamoto; Figure 1 Item 21c).

As per claim 7, Pontius as modified also teaches wherein the converter comprises a Gray-to-Binary converter (Miyamoto; Figure 1 Item 21c).

As per claim 8, Pontius as modified also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn is connected to the FIFO memory.

As per claim 9, Pontius as modified also teaches wherein the read pointer is coupled to the FIFO memory via a Gray-to-binary converter (Miyamoto; Figure 1 Item 22c).

As per claim 10, Pontius as modified also teaches wherein the code generator is coupled to a read pointer (Miyamoto; Figure 1 Item 22), which in turn, is coupled to the storage device.

As per claim 11, Pontius as modified obviously teaches wherein the storage device comprises a bank of registers because a bank of registers can store information the same way as a FIFO memory device.

As per claim 14, Pontius as modified obviously teaches that the asynchronous FIFO memory comprises a write clock domain and a read clock domain because asynchronous memory devices typically have a read clock domain and an independent write clock domain.

As per claim 15, Pontius as modified obviously teaches that the asynchronous FIFO memory comprises a write clock in the write clock domain, a read clock in the read clock domain, and that the read and write clock are asynchronous to each other because any asynchronous system has separate independent clocks to perform separate operations in different domains that are independently from one another.

As per claim 17, Pontius as modified obviously teaches that reading and writing are asynchronous because asynchronous FIFO memories allow for reading and writing that are controlled by clocks that are independent from each other.

As per claim 18, Pontius as modified teaches that reading and writing are part of a FIFO process (Pontius; Col 4 Lines 37 – 46).

As per claim 19, Pontius as modified teaches that the asynchronous memory is an asynchronous FIFO memory (Pontius; Col 4 Lines 37 – 46).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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